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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/410,974	10/01/1999	ANDREW M. JONES	99-TK-252	7705

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EXAMINER	
PHILPOTT, JUSTIN M	
ART UNIT	**PAPER NUMBER**
2665	18

DATE MAILED: 06/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/410,974	Applicant(s) JONES ET AL.	
	Examiner Justin M Philpott	Art Unit 2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10 and 12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10 and 12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed May 7, 2004 have been fully considered but they are not persuasive.

Specifically, applicant argues that the cited prior art fails to disclose newly added limitations of the amended independent claims, including functional modules that are formed within an integrated circuit. However, as discussed in the following action, these newly added limitations of the amended independent claims are met by the cited prior art. Thus, applicant's argument is not persuasive.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 3, 4, 6, 7, 9, 10, 12-14, 16, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,283,904 to Carson et al. in view of U.S. Patent No. 4,807,116 to Katzman et al.

Regarding claims 1, 6, 7, 9, 10 and 12, Carson teaches a plurality of functional modules (e.g., MPIC 104 in FIG. 2, see also col. 4, line 13 – col. 18, line 35) interconnected via a packet router (e.g., MPIC I/O unit 102), each functional module having packet handling circuitry (e.g., circuitry in FIG. 5 comprising MPIC bus send/receive & arbitration 226) for generating and receiving packets conveyed by the packet router; wherein at least a first set of the functional

modules, acting as initiator modules, have packet handling circuitry which includes request packet generation circuitry for generating request packets (e.g., interrupt request, see col. 5, lines 17-54, specifically lines 44-45) for implementing transactions, each request packet including a destination indicator (e.g., destination, see FIG. 7 and col. 8, line 40 – col. 14, line 63) identifying a destination of the packet and an operation field (e.g., bits 0-17 in FIG. 7) denoting the function to be implemented by the request packet, wherein the operation field comprises a number of bits (0-19) of which a single packet type bit (e.g., trigger mode) denotes the type of packet, three operation family bits denote the function (e.g., delivery mode) to be implemented by the packet and two operation qualifier bits (e.g., remote read status) act to qualify the function. While Carson may not specifically disclose exactly eight bits in the operation field, exactly four operation family bits and exactly three operation qualifier bits, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to utilize a specific other number of bits in Carson, since it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value.

Further, Carson teaches the invention is an improvement over a specific integrated circuit (e.g., Intel's 82C59A and also Intel's 82380, see col. 1, line 57 – col. 2, line 55) comprising functional modules (e.g., 11-14, see FIG. 1). Thus, Carson anticipates that the invention may similarly be exemplified by an integrated circuit comprising the functional modules by teaching that the invention is an improvement over the prior art integrated circuit comprising functional modules. Furthermore, it is generally considered to be within the ordinary skill in the art to shift the location of parts absent a showing of unexpected results. Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to shift the location of any elements from a location outside of a common integrated circuit to a location inside of a common integrated circuit since it is generally considered to be within the ordinary skill in the art to shift the location of parts absent a showing of unexpected results. The contention of obvious choice in design can be overcome if Applicant establishes unexpected results. In re Japikse, 86 USPQ 70 (CCPA 1950). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to include the elements taught by Carson within a common integrated circuit since Carson teaches that the invention is an improvement over the prior art integrated circuit comprising functional modules, and since it is generally considered to be within the ordinary skill in the art to shift the location of parts absent a showing of unexpected results.

However, Carson may not specifically disclose a second set of functional modules acting as target modules generates response packets wherein the single packet type bit distinguishes between request packets and response packets.

Katzman teaches a circuit similar to Carson wherein a plurality of functional modules acting as target modules (e.g., modules 33 in FIGS. 1 and 2, and col. 3, line 45 – col. 49, line 68)

are interconnected via a packet router (e.g., bus controller 37) with each functional module having packet handling circuitry (e.g., inter-processor control 55) for generating and receiving packets conveyed by the packet router. Katzman further teaches generating response packets (e.g., SND ACK in FIG. 7, see also acknowledgement ready signal in col. 74, lines 57-61) wherein a bit distinguishes between a request and a response (e.g., see FIG. 9 wherein SND REQ differs from SND ACK by a bit). The teachings of Katzman provide for a modularized multiprocessor system wherein major components can be removed or replaced without system interruption or modifications to other hardware or software, thus improving flexibility and reducing operator cost (e.g., see col. 3, lines 18-43). Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the teachings of Katzman to the circuit of Carson in order to improve flexibility and reduce operator cost.

Regarding claims 3, 13, 17 and 19, Carson teaches the function in each request packet is a memory access operation including cache operations (e.g., see col. 5, lines 46-50).

Regarding claims 4, 10 and 14, Carson further teaches a physical mode (e.g., see col. 5, line 60 – col. 6, line 6) wherein a unique 8-bit MPIC-ID selects a single destination (i.e., primitive access) or a broadcast to all MPICs (i.e., compound access).

Regarding claim 16, while Carson may not specifically disclose memory access operations include load, store, read-modify-write and swap operations, Examiner takes official notice that such operations are commonly-performed memory operations well known in the art. Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art for the memory access operations of Carson to include load, store, read-modify-write and swap

operations since it is well known in the art that such operations are commonly-performed memory operations.

4. Claims 5, 8, 15, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carson in view of Katzman, further in view of U.S. Patent No. 5,704,034 to Circello.

Regarding claims 5, 8 and 15, Carson in view of Katzman teaches the circuit according to claims 1, 7 and 12 as discussed above, however, Carson in view of Katzman may not specifically disclose the request packets include a data object, the size of which is denoted by the operation qualifier. Circello teaches a circuit for initializing a data processing system which involves sending signals (e.g., processor status PST and data signals DDATA) from a module (e.g., 10 in FIG. 1) to a system (e.g., 7). The signals include a data object (e.g., DDATA) and the size of the data object is denoted by two bits of the PST (i.e., an operation qualifier). Particularly, when a data object is transferred (indicated by bits 3:2 equaling 10, see FIG. 10), the size of the data object is denoted by bits 1:0 (wherein 00, 01, 10, and 11 denote in binary the number of bytes which are to be transferred). In the event transfers of more than four bytes were desired, at the time of the invention it would have been obvious to one of ordinary skill in the art to use additional bits in the operation qualifier (e.g., three) to denote the size of the data object (e.g., DDATA) since it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. Furthermore, applying the teachings of Circello to the system of Carson in view of Katzmans would provide an improved system wherein an element would advantageously be aware of the size of particular data transfers prior to transfer

completion and wherein processor failures can be identified and corrected during normal operation (e.g., see col. 2, lines 44-51). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the teachings of Circello to the system of Carson in view of Katzmans in order to provide an improved system wherein an element would advantageously be aware of the size of particular data transfers prior to transfer completion and wherein processor failures can be identified and corrected during normal operation.

Regarding claims 18 and 20, Circello further teaches four PST bits denoting that the PST (e.g., operation field) is user defined (see FIG. 10, when PST[3:0] equals 0011).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin M Philpott whose telephone number is 703.305.7357. The examiner can normally be reached on M-F, 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D Vu can be reached on 703.308.6602. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Justin M Philpott

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